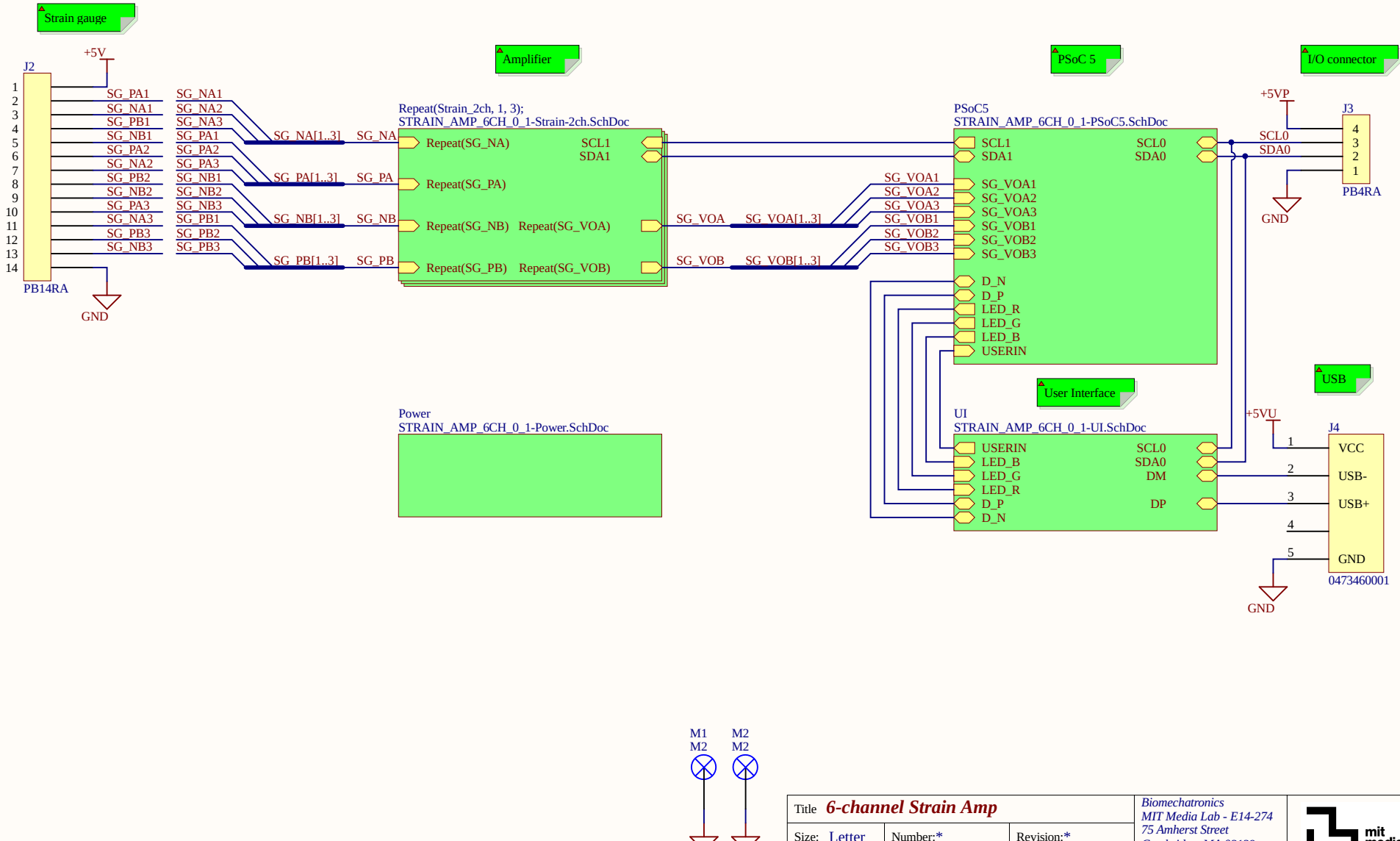
STRAIN_AMP_6CH_0_1
6-channel Strain Gauge Amplifier

- "Fixed" gain of 125 (Possible to change 0603 resistor to modify)
- I²C programmable offset compensation (+V/2 ±20%) - 8 bits
- Output available by I²C and USB (12 to 20bits)
- Non-volatile offset settings
- Common mode input filter to reject EMI perturbation
- 585Hz 2nd Order Low-Pass Filter (-3dB)
- ESD & over-voltage protected IOs
- 5V operation. External I²C is 3V3 by default, but can be 5V.
- Up to 127 sensors per I²C bus
- Can be powered by USB or by the I/O connector.



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Instrumentation Amplifier

Input filter & protection

SG_NA

+5V

R9D 1k

R9C 1k

NA

C16D 100nF

C16C 100nF

D1A TPD4E004DRYR

IO1

IO2

GND GND GND

SG_PA

+5V

R9B 1k

R9A 1k

PA

C16B 100nF

C16A 100nF

D1B TPD4E004DRYR

IO1

IO2

GND GND GND

R8 240k

±0.1%

R10 10k

VRA

U3A

1 RGASHDNA

12 REFA VoutA

2 Vin-A

3 Vin+A

INA2331

14 +5V

13 SG_VOA

2.7 to 5.5V

G = 125, could be 5 < G < 1000

Cascaded LPF 1.6kHz made with networks to get the best matching possible

Digital pot.

Assemble channels differently!

U2A MCP4661T-103

SCL1

SDA1

16 HVC/A0

1 SCL

2 SDA

15 VDD

VSS

EP

3 NC

14 A1

13 A2

12 WP

11

+5V +5V +5V

R2 DNS

R3 DNS

A1

A2

R19 0

R20 0

0b0101[A2][A1]0

2.7 to 5.5V

GND GND GND GND

Instrumentation Amplifier

Input filter & protection

SG_NB

+5V

R13D 1k

R13C 1k

NB

C19D 100nF

C19C 100nF

D1C TPD4E004DRYR

IO1

IO2

GND GND GND

SG_PB

+5V

R13B 1k

R13A 1k

PB

C19B 100nF

C19A 100nF

D1D TPD4E004DRYR

IO1

IO2

GND GND GND

R12 240k

±0.1%

R15 10k

VRB

U3B

7 RGBSHDNB

10 REFB VoutB

6 Vin-B

5 Vin+B

INA2331

8 +5V

9 SG_VOB

2.7 to 5.5V

G = 125, could be 5 < G < 1000

Cascaded LPF 1.6kHz made with networks to get the best matching possible

Offset adj.

+5V

R11 7.5k

VRA

U2B MCP4661T-103

P1A

P1W

P1B

7 6 5

PRA 3

U4A MCP6002

2 1

R14 7.5k

C18 100nF

+V/2 ±20%

GND GND

U3C INA2331

11 V+

4

+5V

U4C MCP6002

8

4 EP

GND

GND

+5V

R16 7.5k

VRB

U2C MCP4661T-103

P0A

P0W

P0B

8 9 10

PRB 5

U4B MCP6002

6 7

R17 7.5k

C20 100nF

+V/2 ±20%

GND GND

Decoupling

+5V +5V +5V +5V

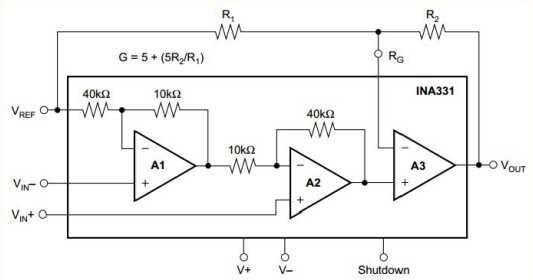
C15 100nF

C21 100nF

C22 100nF

C23 10nF

GND GND GND GND



Low-noise wiring:
==========
- Add a shield to the cable. Link it to GND on the Strain Amp.
- Make two twisted pair: excitation wires and signal wires

For all the details please refer to http://www.vishaypg.com/docs/11051/tn501.pdf

Title	**Dual Strain Amplifier**		
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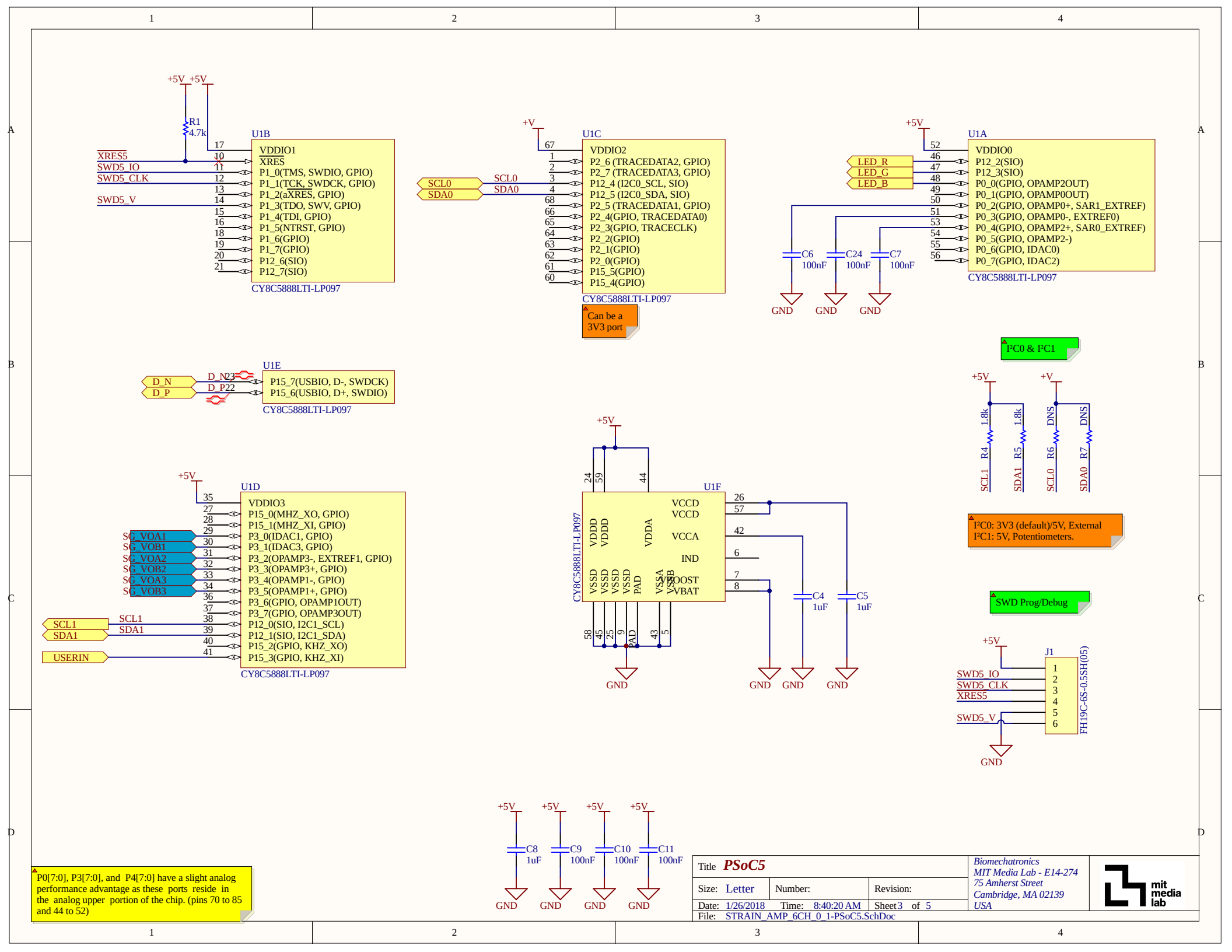
+5V +5V
R1
4.7k
U1B
VDDIO1
XRES
P1_0(TMS, SWDIO, GPIO)
P1_1(TCK, SWDCK, GPIO)
P1_2(aXRES, GPIO)
P1_3(TDO, SWV, GPIO)
P1_4(TDI, GPIO)
P1_5(NTRST, GPIO)
P1_6(GPIO)
P1_7(GPIO)
P12_6(SIO)
P12_7(SIO)
XRES5
SWD5_IO
SWD5_CLK
SWD5_V
CY8C5888LTI-LP097
+V
U1C
VDDIO2
P2_6 (TRACEDATA2, GPIO)
P2_7 (TRACEDATA3, GPIO)
P12_4 (I2C0_SCL, SIO)
P12_5 (I2C0_SDA, SIO)
P2_5 (TRACEDATA1, GPIO)
P2_4(GPIO, TRACEDATA0)
P2_3(GPIO, TRACECLK)
P2_2(GPIO)
P2_1(GPIO)
P2_0(GPIO)
P15_5(GPIO)
P15_4(GPIO)
SCL0
SDA0
CY8C5888LTI-LP097
Can be a 3V3 port
+5V
U1A
VDDIO0
P12_2(SIO)
P12_3(SIO)
P0_0(GPIO, OPAMP2OUT)
P0_1(GPIO, OPAMP0OUT)
P0_2(GPIO, OPAMP0+, SAR1_EXTREF)
P0_3(GPIO, OPAMP0-, EXTREF0)
P0_4(GPIO, OPAMP2+, SAR0_EXTREF)
P0_5(GPIO, OPAMP2-)
P0_6(GPIO, IDAC0)
P0_7(GPIO, IDAC2)
LED_R
LED_G
LED_B
C6 100nF
C24 100nF
C7 100nF
GND
CY8C5888LTI-LP097
U1E
P15_7(USBIO, D-, SWDCK)
P15_6(USBIO, D+, SWDIO)
D_N
D_P
CY8C5888LTI-LP097
I²C0 & I²C1
+5V
+V
1.8k
R4
R5
DNS
R6
R7
SCL1
SDA1
SCL0
SDA0
I²C0: 3V3 (default)/5V, External
I²C1: 5V, Potentiometers.
+5V
U1D
VDDIO3
P15_0(MHZ_XO, GPIO)
P15_1(MHZ_XI, GPIO)
P3_0(IDAC1, GPIO)
P3_1(IDAC3, GPIO)
P3_2(OPAMP3-, EXTREF1, GPIO)
P3_3(OPAMP3+, GPIO)
P3_4(OPAMP1-, GPIO)
P3_5(OPAMP1+, GPIO)
P3_6(GPIO, OPAMP1OUT)
P3_7(GPIO, OPAMP3OUT)
P12_0(SIO, I2C1_SCL)
P12_1(SIO, I2C1_SDA)
P15_2(GPIO, KHZ_XO)
P15_3(GPIO, KHZ_XI)
SG_VOA1
SG_VOB1
SG_VOA2
SG_VOB2
SG_VOA3
SG_VOB3
SCL1
SDA1
USERIN
CY8C5888LTI-LP097
+5V
U1F
VCCD
VCCD
VDDD
VDDD
VDDA
VCCA
IND
VSSD
VSSD
VSSD
PAD
VSSA
VBOOST
VBAT
CY8C5888LTI-LP097
C4 1uF
C5 1uF
GND
SWD Prog/Debug
+5V
J1
SWD5_IO
SWD5_CLK
XRES5
SWD5_V
FH19C-6S-0.5SH(05)
GND
+5V
C8 1uF
C9 100nF
C10 100nF
C11 100nF
GND
P0[7:0], P3[7:0], and P4[7:0] have a slight analog performance advantage as these ports reside in the analog upper portion of the chip. (pins 70 to 85 and 44 to 52)
Title PSoC5
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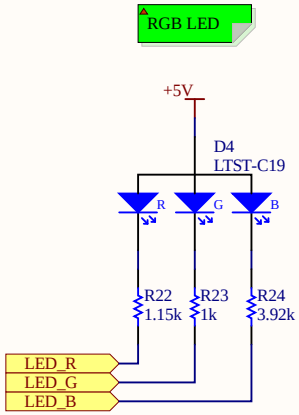

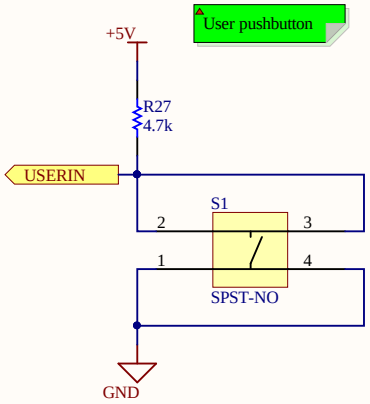

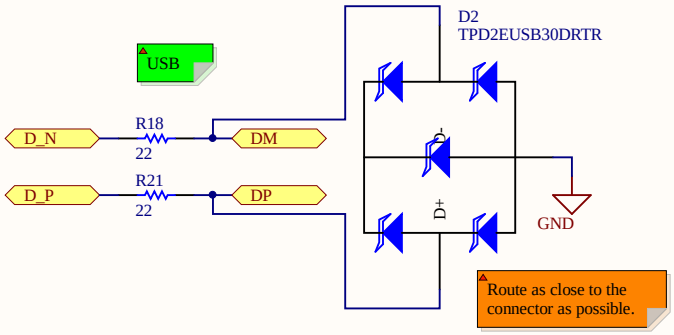

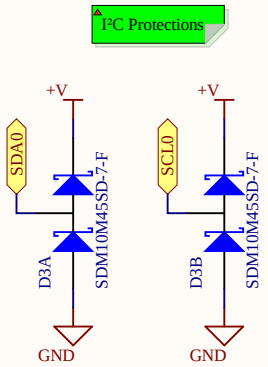

Title	***User Interface***		*Biomechatronics* *MIT Media Lab - E14-274* *75 Amherst Street* *Cambridge, MA 02139* *USA*
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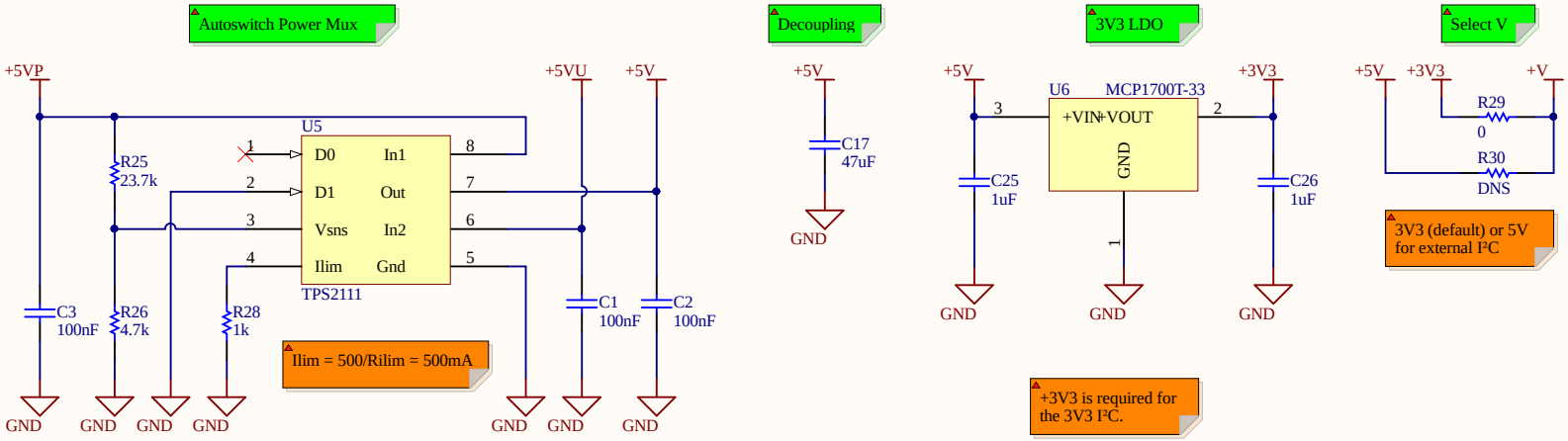
File: STRAIN_AMP_6CH_0_1-UI.SchDoc			



If the +5VP supply is available, it powers the circuit. Otherwise, USB (+5VU) is used.

In the auto-switching mode (D0 = 1, D1 = 0), an internal power FET connects OUT to IN1 if the VSNS voltage is greater than 0.8 V. Otherwise, the FET connects OUT to the higher of IN1 and IN2. The Truth Table illustrates the functionality of VSNS.

With 23.7k & 4.7k it will switch around 4.8V.

Title	***Power***		*Biomechatronics* *MIT Media Lab - E14-274* *75 Amherst Street* *Cambridge, MA 02139* *USA*
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